UNITED STATES PATENT AND TRADEMARK OFFICE

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10/584,733	05/25/2007	Kang-Chan Lee	CU-4904 WWP	8187

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

	Application No.	Applicant(s)
Office Action Summary	10/584,733	LEE ET AL.
	Examiner	Art Unit	
	I-CHAN YANG	2178	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *27 May 2007*.
2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-9* is/are pending in the application.
    4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) *1-9* is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☒ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on *26 June 2006* is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a) ☒ All   b) ☐ Some *   c) ☐ None of:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____.
      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)
1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date *8/18/06; 11/13/06; 7/24/08*.
4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____ .

DETAILED ACTION

This action is responsive to the following communications: application filed on

5/25/2007, of which Claims 1-9 are pending.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 8/18/2006; 11/03/2006; and

7/24/2008 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the

information disclosure statement is being considered by the examiner.

Foreign Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers

have been placed of record in the file.

Title

The title of the invention is not descriptive. A new title is required that is clearly

indicative of the invention to which the claims are directed. Applicant is advised to

amend the title to include the concepts such as independent or specialized hardware

XML processor within a system for XML parsing.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they

include the following reference character(s) not mentioned in the description:

- Fig. 2, reference character 17

- Fig. 3, reference characters 30, 31, 32 and 33

- Fig. 9 & 10, reference characters 30 and 50

The drawings are further objected to for the following:

- Fig. 11, conditional branch 66 should have been checking for whether a parsing tree is necessary (see [65]), rather than "perform by software processor".

- Fig. 11, conditional branch 67 should have been checking for whether fast processing is necessary (see [67]), rather than "perform by software processor".

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities:

- Reference character 13 in line 1 of [36] should have been 15 to be consistent with the drawings.

- Reference character 15 in line 2 of [36] should have been 17 to be consistent with the drawings.

- Reference character 50 in line 3 of [60] should have been 51 to be consistent with the drawings.

Appropriate correction is required.

Claim Objections

Claims 2 and 3 are objected to for the following:

- Regarding claims 2 and 3, the phrase "i.e." renders the claims indefinite because it is unclear whether the limitation(s) following the phrase are part of the claimed invention. See MPEP § 2173.05(d). In the following examination, the immediate limitation following the phrase "i.e." and ending with the semicolon, in Claims 2 and 3, will be construed as having no patentable weight.

- Regarding Claim 3, the phrase "and the like" renders the claim(s) indefinite because the claim(s) include(s) elements not actually disclosed (those

encompassed by "and the like"), thereby rendering the scope of the claim(s)

unascertainable. See MPEP § 2173.05(d).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the

claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the

various claims was commonly owned at the time any inventions covered therein were

made absent any evidence to the contrary. Applicant is advised of the obligation under

37 CFR 1.56 to point out the inventor and invention dates of each claim that was not

commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g)

prior art under 35 U.S.C. 103(a).

Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being obvious over *James*

***et al.* (US 7,013,424, hereinafter, *James*) in view of *Ross* (US 7,305,615).**

As per Claim 1: *James* discloses *an XML processor comprising* (*James*, Col 3, lines

33-42)*:*

> *a first memory storing software for performing an XML processing, variables, and*

values required to execute software (*James*, Fig. 4, storage 430, memory 4[2]8, Col 10,

lines 14-17)*;*

> *a hardware processing module performing a part of the XML processing in a*

hardware manner (*James*, Fig. 4, special purpose processor 432, Col 10, lines 48-56)*;*

and

> *a CPU controlling the XML processing by the software stored in the first memory*

(*James*, Fig. 4, general purpose processor 412, Col 10, lines 14-17)*.*

James does not appear to explicitly disclose

> *a second memory employed by the hardware processing module.*

However, *Ross* discloses

> *a second memory employed by the hardware processing module* (*Ross*, Fig. 5,

parsing accelerator, Fig. 6, memory 601 employed by parsing accelerator, Col 6, lines

46-60)*.*

At the time of the invention, it would have been obvious to one of ordinary skill in the art,

to include additional memory, such as processor cache, in the dedicated XML

processor. The motivation for doing so would have been to further optimize the XML

processing by storing at least a portion of the processing data on the cache and avoid

the more expensive processing time associated with data fetching operations from the

main memory.

As per Claim 2: The combination of *James* and *Ross* discloses *the XML processor*

according to claim 1, wherein the hardware processing module performs a memory

management function used in XML parsing, i.e., assignment, return, and reassignment

of memory among XML processing functions (Col 7, lines 21-23, dedicated XML

processor creates DOM for parsed XML; Col 5, line 63 thru Col 6, line10, DOM creation

includes memory management operations).

Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being obvious over *James*

in view of *Ross* and further in view of *Hind et al.* (US 6,938,204, hereinafter, *Hind*).

As per Claim 3: The combination of *James* and *Ross* discloses *the XML processor*

according to claim 2, wherein the hardware processing module processes assignment,

reassignment, and return of memory with respect to XML elements which are expressed

as nodes and a tree relation between the nodes (*James*, Col 6, lines 1-10, memory

allocation, de-allocation, and reclamation for objects within XML hierarchical structure).

The combination of *James* and *Ross* does not appear to explicitly disclose

a node usage check table divided into several blocks, each block indicating

whether to use a corresponding node table;

a node table managing the whole information that each node has to store, i.e., a

node name, a node type, a parent node, a child node, and the like; and

a node memory storing actual content of every component of the node table.

However, *Hind* discloses an array based storage format for XML data, and further

discloses

a node usage check table divided into several blocks, each block indicating

whether to use a corresponding node table (*Hind*, Fig. 5C, 520, Col 13, lines 26-36, the

attribute array is a node usage check table divided into several blocks, each block

indicating whether a corresponding secondary array is used);

a node table managing the whole information that each node has to store, i.e., a

node name, a node type, a parent node, a child node, and the like (*Hind*, Fig. 5C, 530

and 540, Col 13, lines 36-40, the secondary array is a node table managing the whole

attribute information each node has to store); *and*

a node memory storing actual content of every component of the node table (Fig.

5C, Fig. 4C, Col 13, line 54 thru Col 14, line 5, data buffer 480 in Fig. 4C is a node

memory storing actual content of every component from the secondary array).

At the time of the invention, it would have been obvious to one of ordinary skill in the art,

to include *Hind*'s array-based storage format for XML data in the combination of *James*

and *Ross*. The feasibility and desirability of such combination is further evident in the

incorporation of *Hind* by reference in the Specification of *James* (*James*, Col 6, lines 25-

30). The motivation for the combination would have been to realize further performance

gains by implementing the array-based processing for faster navigation of the tree

structure (*James*, Col 6, lines 11-25).

As per Claim 4: The combination of *James, Ross,* and *Hind* discloses *the XML*

processor according to claim 3, wherein the node table has addresses in which every

component on the node memory is respectively stored (*Hind*, Col 13, lines 40-50,

secondary array has references/addresses in the form of a data buffer pointer, a offset

from the beginning of the data buffer, and a data length for every attribute component).

Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being obvious over *James*

in view of *Ross* and further in view of *Dapp et al.* (US 7,080,094, hereinafter,

***Dapp*).**

As per Claim 5: The combination of *James* and *Ross* does not appear to explicitly

disclose

> *wherein the hardware processing module performs an XML DTD processing.*

However, *Dapp* discloses a hardware XML processing module that performs XML DTD

processing (*Dapp*, Col 3, lines 27-28, hardware XML accelerator, Col 2, lines 18-25,

DTD or XML schema validation).

At the time of the invention, it would have been obvious to one of ordinary skill in the art,

to perform DTD processing with the dedicated XML processor. The motivation for doing

so would have been to use a specialized XML processor for resource-intensive XML

validation operations (*Dapp*, Col 2, line 55 thru Col 3, line 2).

As per Claim 6: The combination of *James* and *Ross* does not appear to explicitly

disclose

> *wherein the hardware processing module performs a state machine of an XML*

schema.

However, *Dapp* discloses a hardware XML processing module that *performs a state*

machine of an XML schema (*Dapp*, Col 2, lines 37-41).

At the time of the invention, it would have been obvious to one of ordinary skill in the art,

to perform XML validation processing including state machine implementation with the

dedicated XML processor. The motivation for doing so would have been to use a

specialized XML processor for resource-intensive XML validation operations (*Dapp*, Col

2, line 55 thru Col 3, line 2).

Claims 7-9 are rejected under 35 U.S.C. 103(a) as being obvious over *James* in view of *Uchida* (US 2005/0034032) and further in view of *Dapp.*

As per Claim 7: *James* discloses *an XML processing method performed in a system having an independent hardware-based first XML processor and a software-based second XML processor, the method comprising:*

performing an XML processing by the second XML processor (*James*, Col 3, lines 33-42 and lines 59-65, dedicated processor includes a software-based general purpose processor for processing XML); *and*

performing an XML processing by the first XML processor (*James*, Col 3, lines 33-58, dedicated processor includes a hardware-based special purpose processor).

James does not appear to explicitly disclose

checking a size of an XML file to be processed; performing an XML processing by the second XML processor if a size of the XML file to be processed is larger than an established size; and performing an XML processing by the first XML processor if a size of the XML file to be processed is not larger than the established size.

However, *Uchida* discloses checking the size of an XML file to be processed to avoid data overflow due to oversized XML documents unsupported by the system resources. Accordingly, XML files smaller than an established size will be processed, while XML

files larger than an established size will generate errors (*Uchida*, Fig. 5, Steps 14-19,

[0036], lines 1-4 preventing data overflow, [0071], checking the size of XML document).

And *Dapp* discloses processing the XML file with a software-based general purpose

processor when the complexity of the XML file exceeds the capacity of a special

purpose, hardware-based processor (*Dapp*, Col 3, lines 3-23).

At the time of the invention, it would have been obvious to one of ordinary skill in art, to

include in the XML processing method of *James*, additional steps of: checking the size

of the XML file; processing the XML file with a software-based general processor if the

file size exceeds the capacity supported by a hardware-base special purpose

processor; and processing the XML file with a hardware-based special purpose

processor if otherwise. The motivation for the inclusion would have been to avoid

undesirable performance or risk associated with processing with a hardware-based

special purpose processor beyond capacity.

As per Claim 8: The combination of *James*, *Uchida*, and *Dapp* does not appear to

explicitly disclose

   checking whether establishment of a tree is necessary after the XML processing;

performing the XML processing by the second XML processor if the establishment of

the tree is not necessary; and performing the XML processing by the first XML

processor if the establishment of the tree is necessary.

However, *James* discloses performing conventional XML processing with software

executing on a general purpose processor (*James*, Col 2, lines 52-61). *James* further

discloses the establishment of a DOM tree during XML processing is computationally

expensive in terms of processing time and memory requirements (*James*, Col 5, lines

63-67). *James* further discloses a special purpose hardware-based processor for

alleviating the load on the general purpose processor and for performing efficient XML

processing on traditionally resource-intensive operations (*James*, Col 3, lines 22-42).

At the time of the invention, it would have been obvious to one of ordinary skill in the art,

with the teachings of *James*, *Uchida*, and *Dapp* in front of him or her, to include

checking whether a resource-intensive DOM building processing is needed, and

offloading the DOM building to a special purpose processor if desired. The motivation

for the inclusion would have been utilize a dedicated processor for XML processing

operations traditionally performed by the general purpose processor for faster and more

efficient XML processing.

As per Claim 9: The combination of *James*, *Uchida*, and *Dapp* discloses *the method*

according to claim 7, further comprising:

     checking whether a fast processing is necessary (performing XML processing

with the dedicated processor inherently includes determining by an user that fast

processing is necessary);

performing the XML processing by the second XML processor if the fast

processing is not necessary (James, Col 2, lines 52-61); and

performing the XML processing by the first XML processor if the fast processing

is necessary (James, Col 3, lines 33-42).

References

All prior art made of record in this Office Action or as cited on form PTO-892

notwithstanding being relied upon, is considered pertinent to applicant's disclosure.

Therefore, applicant is required under 37 CFR 1.111(c) to consider these references

fully when responding to this Office Action.

- US 2004/0083466   hardware parser accelerator

- US 2004/0088262   TCP/IP offloading if fast processing required

- US 2004/0221229   data structures related to documents

- US 2005/0138381   dynamic content security processor for XML

- US 2006/0106837   integral parser

- US 2006/0236224   XML offload processor

- US 2006/0265689   processing XML in a network

- US 2007/0016554   hardware accelerated validating parser

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to I-Chan Yang whose telephone number is (571) 270-

3840. The examiner can normally be reached on Monday - Thursday, 9:00 a.m. - 5:00

p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Stephen Hong can be reached on (571) 272-4124. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For

more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business

Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO

Customer Service Representative or access to the automated information system, call

800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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